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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,035	07/23/2001	Paul C. Davis	23	3476
7590	04/07/2004		EXAMINER	
Ryan, Mason & Lewis, LLP 90 Forest Avenue Locust Valley, NY 11560			VU, QIANG D	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/911,035	DAVIS, PAUL C.
	Examiner Quang D Vu	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12 January 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 2-17,30 and 31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 2-17,30 and 31 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date: _____
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____ 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2-17, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,225,674 to Lim et al. in view of US Patent No. 5,631,572 to Sheen et al.

Regarding claim 30, Lim et al. (figures 1-20) teach an integrated circuit, comprising:

a first circuit section (15) formed in a substrate (11, 14);

a second circuit section (16) formed in the substrate (11, 14), the second circuit section

being spaced laterally from the first circuit section;

an isolation buried layer (12) formed under at least a portion of the first circuit section (15); and

a conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12). It is inherent that the conductive layer (112) reducing an effective lateral resistance of the isolation buried layer (12).

Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. However, Sheen et al. teach a connection of one net of conductive traces (column 10, lines 24-28). Therefore, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to incorporate the teaching of Sheen et al. into the device taught by Lim et al. because it depends on the amount of noise that need to be reduced. The combined device shows the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

Regarding claim 2, Lim et al. teach a plurality of conductive plugs (33) formed in the substrate (11, 14), the plugs (33) providing a substantially low resistance path for electrically connecting the conductive layer (112) to the isolation buried layer (12).

Regarding claim 3, Lim et al. (figures 1-20) teach an integrated circuit, comprising:
a first circuit section (15) formed in a substrate (11, 14);
a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;
an isolation buried layer (12) formed under at least a portion of the first circuit section (15); and

a conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12) at a plurality of points spaced throughout the buried layer. It is inherent that the conductive layer (112) reducing an effective lateral resistance of the isolation buried layer (12) to thereby increase an electrical isolation between the first (15) and second circuit (16) sections.

Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. However, Sheen et al. teach a connection of one net of conductive traces (column 10, lines 24-28). Therefore, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to incorporate the teaching of Sheen et al. into the device taught by Lim et al. because it depends on the amount of noise that need to be reduced. The combined device shows the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

Regarding claim 4, the combined device shows the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net.

Regarding claim 5, the combined device shows the net overlays at least a portion of the first circuit section.

Regarding claim 6, Lim et al. teach the isolation buried layer (12) is connected to a ground (column 8, lines 51-55).

Regarding claim 7, Lim et al. teach the conductive layer (112) is formed at least in part of metal (column 8, lines 29-30).

Regarding claim 8, Lim et al. teach a second isolation buried layer (13) formed under at least a portion of the second circuit section (16); and a second conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer (13).

It is inherent that the second conductive layer (112) reducing an effective lateral resistance of the second isolation buried layer (13).

Regarding claim 9, Lim et al. teach a plurality of conductive plugs (38) formed in the substrate (11, 14), the plugs (38) providing a substantially low resistance path for electrically connecting the second conductive layer (112) to the second isolation buried layer (13).

Regarding claim 10, the combined device shows the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

Regarding claim 11, the combined device shows the second net includes a plurality of holes therein, wherein at least a portion of the first circuit section being formed in one or more holes in the net.

Regarding claim 12, the combined device shows the second net overlays at least a portion of the first circuit section.

Regarding claim 13, Lim et al. teach the first and second conductive layers (112) are electrically connected to separate ground (column 8, lines 51-55).

Regarding claim 14, Lim et al. teach the second circuit section (16) comprises at least one bipolar transistor device, the bipolar transistor device including a collector buried layer (20) formed in the substrate (11, 14) above the second isolation buried layer (13) (see figure 20).

Regarding claim 15, Lim et al. teach the integrated circuit is a mixed signal integrated circuit (column 9, lines 20-22); the first circuit section (15) comprises an IGFET (column 2, lines 19-20); and the second circuit section (16) comprises a bipolar transistor (column 2, lines 21-23).

It is inherent that the IGFET formed in a digital circuit section. It is inherent that the bipolar transistor formed in an analog circuit section.

Regarding claim 16, Lim et al. teach the isolation buried layer (12) has a lower resistivity than the substrate (11).

Regarding claim 17, Lim et al. and Sheen et al. differ from the claimed invention by not showing the isolation buried layer is formed in the substrate at depth in a range from about 2

micrometers to about 5 micrometers from an upper surface of the substrate. It would have been obvious to one having ordinary skill in the art at the time of the invention was made for the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers to about 5 micrometers from an upper surface of the substrate, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 31, Lim et al. teach an integrated circuit, comprising

- a first circuit section (15) formed in a substrate (11, 14);
- a second circuit section (16) formed in the substrate (11, 14), the second circuit section being spaced laterally from the first circuit section;
- a first isolation buried layer (12) formed under at least a portion of the first circuit section (15);
- a first conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12);
- a second isolation buried layer (13) formed under at least a portion of the second circuit section (16); and
- a second conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer (13).

It is inherent that the conductive layer (112) reducing an effective lateral resistance of the first isolation buried layer (12).

It is also inherent that the second conductive layer (112) reducing an effective lateral resistance of the second isolation buried layer (13).

Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net. However, Sheen et al. teach a connection of one net of conductive traces (column 10, lines 24-28). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sheen et al. into the device taught by Lim et al. because it depends on the amount of noise that need to be reduced. The combined device shows the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

Response to Arguments

Applicant's arguments with respect to claims 2-17, 30 and 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
April 2, 2004

Christopher
Primary Examiner

